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PATENT APPLICATION
DOCKET NO.: 200208999-2

REMARKS

Claims 1-6, 9-32, 35 and 36 are presented for examination, of which claims 1, 16 and 27 are in independent form.

Claims 1, 16 and 27 are amended by way of the present response. Additionally, claims 7, 8, 33 and 34 are cancelled without prejudice, limitation or estoppel.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Claim Rejections - 35 U.S.C. §102(b)

Claims 1-36 are rejected in the pending Office Action under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,887,003 to Ranson et al. (hereinafter the *Ranson* reference). In connection with these rejections, the Examiner has commented as follows with respect to base claim 1:

> Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the GPPC comprising:
>
> an AND/OR circuit connected to receive the debug data (col. 12, lines 30-62);
>
> a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated, causes the counter circuit to increment a

current count value (col. 15, lines 56-67 to col. 16, lines 1-39); and

a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a designated relationship to a compare value (col. 12, lines 30-62; col. 11, lines 9-2 1; col. 15, lines 27-55; col. 19, lines 18-67; col. 20, lines 1-14),

wherein the AND/OR circuit activates the increment signal responsive to one or more selected bits of an events signal being set (col. 15, lines 56-65; col. 16, lines 16-39).

The Examiner has further commented the following with respect to claims 7 and 8, the subject matter of which has been incorporated into base claim 1:

Referring to claim 7, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ('GPPC") connected to a bus carrying debug data wherein, when the AND/OR circuit is operating in AND mode, the AND/OR circuit activates the increment signal when all of the selected bits of the events signal are set (col. 15, lines 27-55).

As to claim 8, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein when the AND/OR circuit is operating in OR mode, the AND/OR circuit activates the increment signal when at least one of the selected bits of the events signal is set (col. 15, lines 27-55).

Applicant respectfully submits that the pending §102(b) rejections of the claims have been overcome or otherwise rendered moot by the present response. As set forth in base claim 1, an embodiment of the present patent application is directed to a general purpose performance counter connected to a bus carrying debug data. The general purpose performance counter comprises, *inter alia*, an AND/OR circuit connected to receive an events signal that comprises the debug data. The AND/OR circuit also sends an increment signal to a counter circuit. When the AND/OR circuit is operating in OR mode, the AND/OR circuit activates the increment signal responsive to one or more selected bits of the events signal being set and when the AND/OR circuit is operating in AND mode, the AND/OR circuit activates the increment signal when all of the selected bits of the events signal are set.

Similar limitations are found in base claim 16 (directed to another embodiment of a general purpose performance counter) and base claim 27 (directed to an embodiment of a method of implementing a general purpose performance counter).

The *Ranson* reference is directed to a scheme for comparing a group of multi-bit binary fields with a multi-bit expected

pattern to generate a set of final match results. For each multi-bit binary field, *Ranson* compares the field with the expected pattern, generates mask results that select the desired portion of the result, and creates preliminary match results equal to a logical ANDing of all bits making up the bitwise mask result. Secondary match results may be generated by negating all of the preliminary match results and final match results are generated by individually gating all of the secondary match results with separate enable indicators. See Abstract.

Applicant respectfully submits that the *Ranson* reference does not meet all of the limitations of the AND/OR circuit as currently recited in the base claims. It appears that the Examiner has attempted to apply various unrelated circuit portions of *Ranson* in order to show the specific aspects of the claimed AND/OR circuit. The first occurrence of the AND/OR circuit in the claims (i.e., an AND/OR circuit connected to receive the debug data) is read on column 12, lines 30-62. This paragraph describes FIG. 6 and discloses details of a control register. The second occurrence of this same circuit (i.e., wherein the AND/OR circuit activates the increment signal

responsive to the setting of one or more selected bits) is read rather broadly on column 15, line 56 through column 16, line 39. This excerpt describes a programmable state machine entry (FIG. 12), counters (FIG. 13) and a detail of a single counter (FIG. 13). In the *Response to Arguments* section of the pending office action, FIGS. 13 and 14 are again cited, apparently reading three bits input to a counter from increment data bus 1112 as the increment signal. When the AND/OR circuit was recited in claims 7 and 8 (now incorporated into claim 1), the state machine of FIG. 12 is cited; the state machine produces an entirely different signal designated "HIT".

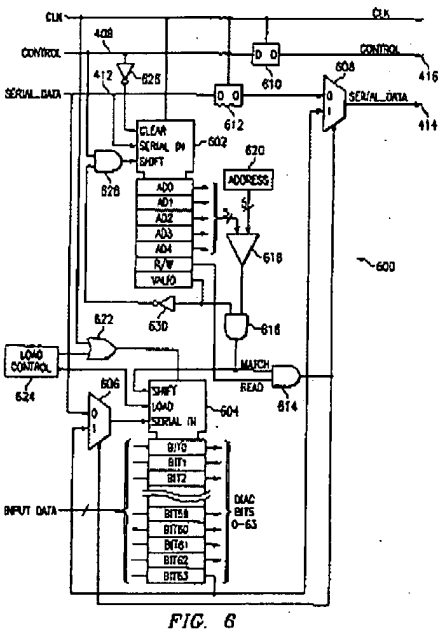


FIG. 6

Looking first at FIG. 6, reproduced herein for convenience, control register 600 receives input data in the lower left corner, which the pending Office Action appears to have equated with the debug data, but the control register circuit does not produce an increment signal that in the OR mode is activated

responsive to one or more selected bits of the events signal (which is now defined as including the debug data) being set and in the AND mode is activated responsive to all of the selected bits of the events signal being set.

In the circuits of FIGS. 13 and 14, reproduced herein for convenience, FIG. 13 discloses a group of counters and FIG. 14 discloses a detail of an individual counter. In FIG. 14, the contents of the three-bit signal from the increment data bus 1112 will, under the right conditions, be added to the counter, but the citation is not clear whether this signal is intended to be equated with the claimed data bus, which is input to the AND/OR circuit, or the increment signal, which is output from the AND/OR circuit. If this is intended to be equated with the increment signal, there is no disclosure that in the OR mode this increment signal is activated

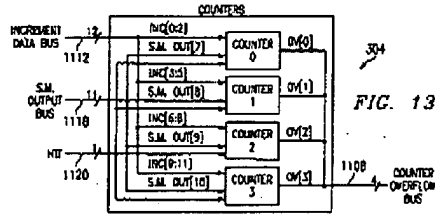
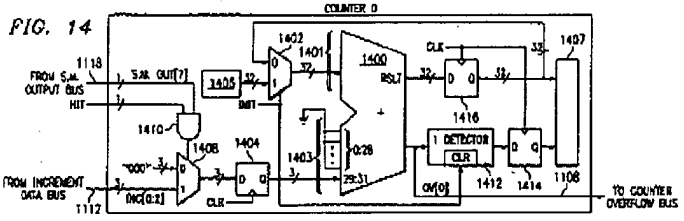


FIG. 13

FIG. 14



responsive to one or more selected bits of the events signal being set and that in the AND mode this increment signal is activated responsive to all of the selected bits of the events signal being set.

In FIG. 12 of *Ranson*, also reproduced herein for convenience, the HIT signal to the counter is active when the state machine is in the present state (i.e., the contents of present state bus is equal to the contents of storage block 1201) and all of the selected bits of state machine inputs bus 1110 are set. This circuit is not able to activate the HIT signal responsive to one or more of the selected bits being set, as is recited for the OR mode in the base claims.

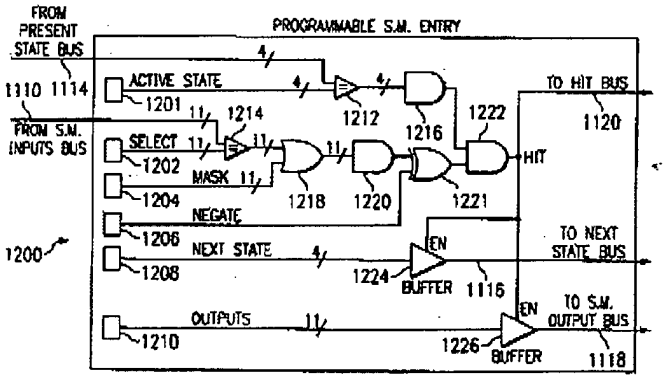


FIG. 12

None of the cited excerpts of *Ranson* provides a teaching or suggestion of an AND/OR circuit that receives debug data and that in the OR mode activates an increment signal when one or more

selected bits are set and in the AND mode activates the increment signal when all of the selected bits are set.

Based on the foregoing, Applicant respectfully submits that base claims 1, 16 and 27 are not anticipated or suggested by the applied art of record, and are therefore in condition for allowance. Claims 2-6 and 9-15 depend from base claim 1, claims 17-26 depend from claim 16, and claims 28-32, 35 and 36 depend from base claim 27, each of the dependent claims introducing additional limitations therein. Accordingly, these dependent claims are also believed to be allowable.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims and in further view of the above remarks and/or amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

Dated: April 3, 2008

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